1. The clock pulses shown are applied to the JK flip-flop clock input. Sketch output $Q$.

![Diagram of JK flip-flop](image1)

2. The clock pulses on next page are applied to the JK flip-flop clock input. Sketch output $Q_1$ & $Q_2$ on next page.

![Diagram of JK flip-flop with clock pulses](image2)
3. Prove the below circuit is a 10-counter.
Objective

Study a JK flip-flop and examine the use of JKS as a binary counter.

Workbench Equipment

- Digital Oscilloscope, Agilent 54621A
- Function Generator, Agilent 33120A
- DC Power Supply, Agilent E3640A

Check-out Equipment, 20-111 window

- Large Breadboard
- Scope Probe (10:1), 2
- Banana to grabber 1 pair, red / black
- BNC to grabber lead
- Heathkit Circuit Design Trainer (use LEDs only)

Background

JK Flip-Flop

The JK flip-flop has several advantages over the RS flip-flop. First, there isn’t an ambiguous state in the JK truth table (see Figure 7-1). In addition, the JK flip-flop is an edge-triggered device and therefore JKS can be easily synchronized by connecting clock inputs together.

Lastly, JK flip-flops have a toggle state. When in toggle mode, the outputs of a JK will equal their opposite state on every high to low (trailing-edge) transition of the clock (CLK) input. The toggle state makes the JK flip-flop very suitable for use in binary counters.

Binary Counters

JKs are often used in binary counters since the output frequency of a JK will be half the CLK input frequency when in toggle mode. JKS connected in “cascade” (output of one JK connected to CLK input of another JK), as shown in Figure 7-2, have output states that increment in binary for every INPUT pulse. Figure 7-2 is an example of an 8-counter, there are eight distinct binary states (000 to 111) at the JKS Q outputs. Note binary count recycles to 000 after 111.
Asynchronous & Synchronous Counters
The counter of Figure 7-2 is asynchronous (not synchronized) since the clock (CK) inputs are not connected together. Synchronized counters have their clock inputs connected together as Figure 7-3 shows. When synchronized, JK outputs are determined by their input conditions at the same time. In this experiment both asynchronous and synchronous counters are demonstrated.

The counter of Figure 7-3 is a 4-counter, i.e. binary states 00, 01, 10 and 11 are possible Q outputs. As can be deduced from the counters of Figures 7-2 (a) and 7-3, there is a $2^N$ relation between the number of counter binary states and the number of JK flip-flops ($N$ = number of JKS). For instance, 4JKs are needed for a 16-counter (0000 to 1111), 5JKs for a 32-counter (00000 to 11111), 6JKs for a 64-counter (000000 to 111111) and so on.

Synchronous counters larger than a 4-counter require additional logic (AND gates), however $2^N$ asynchronous counters do not require additional logic. To make a counter that is something other than a $2^N$ counter, 10-counter for example, additional logic is necessary as will be demonstrated in procedure 3 of this experiment.
74107 JK Flip-Flop Important Information

Pin Diagram:

Operational Notes:

Input signals must never exceed $V_{CC}$, nor fall below ground.

Unused TTL inputs “float” high. This means that if an input is unconnected, the gate will interpret this input as a high or ‘1’ input. If, however, the input is supposed to be fixed at a high state, it should be connected to $V_{CC}$.

Although it is not always shown explicitly on diagrams, a 0.01 to 0.1 μF decoupling capacitor should be used in each circuit. It must have short leads, be connected from $V_{CC}$ to ground, and be as near as possible to the IC. The purpose of this capacitor is to prevent high frequency noise from damaging the IC, or affecting results.

Avoid using long wires in circuits because they contribute to stray capacitance and can adversely affect results.

Make sure to apply $V_{CC}$ to pin 14 and ground to pin 7. If you reverse the Vcc and ground connections the IC will burn.

Procedure 1: JK Flip-Flop

- Select one JK flip-flop of the 74107 IC and connect in toggle mode as shown in prelab #1. Use Agilent E3640A power supply for $V_{CC} = +5V$.
- Use function generator (Hi Z mode) to apply a 0 to 4V 400Hz square wave with a 50% duty cycle.
  - Duty cycle refers to the amount of time a square wave is equal to its largest amplitude (4V in this case) compared to its period.
- Observe on scope Q output and CLK input, capture scope image and record frequency.
  
  \[
  Q\text{ output frequency} = \text{_______ Hz which is approximately _____ X CLK input frequency}
  \]
- While observing both the Q output and clock input on the scope, vary the duty cycle of the clock input between 20% and 80%.
  - Be prepared to explain observation as a postlab question.
- Observe both Q outputs on scope and verify the Q output is 180° out of phase with Q.
Procedure 2: Synchronous Counter

- Build the synchronous counter of Figure 7-3. Again, use Agilent E3640A power supply for \( V_{cc} = +5V \). Connect ground of +5V source to ground of LED box.
- Connect LEDs to Q outputs to visually show binary count.
- Apply 0 to 4V square wave at 1Hz to CLK input.
- Obtain instructor verification that your counter functions correctly.

Instructor Initials: ________

Procedure 3: Asynchronous Counters

- Build an asynchronous 16-counter (see Figure 7-2 (a) for guidance).
- Connect LEDs to Q outputs to visually show binary count.
- Apply 0 to 4V square wave at 1Hz to CLK input.
  - Once certain 16-counter functions as it should proceed to next step.
- Connect a NAND gate to your circuit as shown in prelab #3.
- Obtain instructor verification that your 10-counter functions correctly.

Instructor Initials: ________

- Disconnect NAND gate completely from circuit and connect LEDs to \( \overline{Q} \) outputs instead of Q outputs.
- Binary count should now decrement with every clock pulse, i.e. down-counter.
- Obtain instructor verification that your down-counter functions correctly.

Instructor Initials: ________

Discussion

1. The JK flip-flops used in this experiment have active ______ clears.
2. What type of triggering is used by the JK flip-flops, negative or positive?
3. For a J-K flip-flop, how could you most easily obtain a signal 180° out of phase with the Q output?
4. In procedure 1, how does the Q output frequency compare to the clock input frequency?
5. In procedure 1, what effect did changing the duty cycle have on the output signal of the flip-flop? Why? Hint: A major use of a toggling flip-flop is to obtain a 50% duty cycle pulse, regardless of the input duty cycle.
6. How many JK flip-flops are needed to make a counter that counts from 0 to 255?
7. Draw an asynchronous counter that counts from zero to one hundred twenty.